

SrTiO₃/BaTiO₃ multilayers thin films for integrated tunable capacitors applications

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Available online 9 March 2007

Abstract

In this study, we propose to observe STO/BTO multilayers as tunable dielectric. These layers are deposited onto platinized Si substrate as they are dedicated to be integrated in microelectronic technologies. STO and BTO are deposited by ion beam sputtering (IBS). The number of STO/BTO bilayer, called period in the following, ranges from 1 to 5 with thicknesses in the 65–85 nm range. After Pt top electrode deposition, samples are annealed at temperatures between 300 and 700 °C. High dielectric constant value, correlated with perovskite structure, appears after a 450 °C annealing which is very interesting for above IC integration. SIMS shows weak interdiffusion in the stack after annealing. Dielectric constant increases from 56 to 102 as periods increase from 1 to 5. Simultaneously, tuning range gains 150% with period increasing. Temperature stability and ferroelectric behaviour also increases with periods increase. A curious drawback is apparition of holes in BTO layers after annealing, as observed by TEM.

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Keywords: Films; Interfaces; Dielectric properties; STO/BTO; Perovskite

1. Introduction

Barium titanate (BTO) is one of the most studied ferroelectric materials today. A large number of works were performed on it, and particularly on its solid solution with strontium titanate (STO), the BST,¹ which is widely used for RF and microwave applications for its high tuning range.² Tabata et al. proved that another way to improve dielectric properties is to add a stress into the lattice, by stacking elements with different lattice constant, such as BTO and STO.³

First STO/BTO superlattices were deposited by Iijima et al. by reactive evaporation.⁴ Others multilayers were deposited by sol–gel method,^{5,6} MOCVD,⁷ sputtering,⁸ atomic layer epitaxy,⁹ and PLD.¹⁰ Shimoyama et al.¹¹ also developed an atomic layer epitaxy method, with low oxygen pressure (below 10^{−8} Pa).

A large number of authors studied the influence of the periods on dielectric constant.^{3,5,7,8,10} Tabata et al.¹⁰ noticed that

when the thickness of each layer becomes as large as an atomic layer, the material can be considered as a solid solution of Ba_{0.5}Sr_{0.5}TiO₃, and the dielectric constant dramatically reduced. Some authors showed that multilayers STO/BTO exhibit better dielectric properties than STO, BTO or BST thin films,^{3,10,12} whereas others obtained contradictory results.^{5,13} Koebernik et al.¹³ noticed that multilayer films had better voltage linearity than solid solution of BST. All those results are often contradictory and not yet totally understood. Complementary experiment and analyses are needed for a better comprehension.

In this study, we deposited STO/BTO films by ion beam sputtering (IBS) onto platinized Si substrates and compared their structural and dielectric properties. Devices were patterned on 100 mm wafers.

2. Experiment

The SrTiO₃ and BaTiO₃ layers are deposited alternately by ion beam sputtering. BTO and STO material were previously optimized according to stoichiometric composition, which was checked by RBS. The multilayer stack is deposited onto

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Si/SiO₂ 500 nm/TiO₂ 40 nm/Pt 100 nm substrates. Three stacks are tested: 1 period (or bilayer) STO/BTO, 2 periods STO/BTO, and 5 periods STO/BTO. The first layer deposited is STO. Thicknesses of stacks are 75, 85 and 65 nm, respectively, for 1, 2 and 5 periods.

Pt-top electrodes 100 nm thick ($\varnothing = 110 \mu\text{m}$) are sputtered and patterned by lift-off. Samples are annealed at temperatures between 300 and 700 °C, during 30 min under air.

The X-ray diffraction properties are investigated in θ - 2θ geometry. All diffraction diagrams are obtained from Cu K α as incident X-ray beam, the Cu K β being filtered. The step is 0.05° and the counting time on each step is 4 s. Species interdiffusion between layers is studied by secondary ions mass spectroscopy (SIMS) analysis Cameca 5f. The primary ions are Cs⁺ at 2 keV. Microstructure before and after annealing is observed by TEM bright field using a TECNAI02 microscope.

Permittivity, $\tan \delta$ losses and tuning range = $(C_{\text{max}} - C)/C_{\text{max}}$ of all samples are measured as a function of a bias voltage with a HP 4194A impedance analyzer at 100 kHz. Capacitance versus temperature is measured using a HP 4284A impedance analyzer at 100 kHz. Polarization versus electric field is obtained from a modified Tower-Sawyer circuit.

3. Results and discussion

3.1. Structural properties

The X-ray patterns reported in Fig. 1 contain results for 1 and 5 periods annealed at 650 °C. From 1 period diagram, one observes that STO and BTO peaks are present and then that perovskite structure exists for both. Comparison with the bulk lattice parameters shows that the layers are poorly strained. Values obtained are $a_{\text{BTO}} = 4.000 \text{ \AA}$ (0.2% difference with bulk) and $a_{\text{STO}} = 3.893 \text{ \AA}$ (0.3% difference with bulk). The 5 periods plot shows a peak, between BTO bulk and STO bulk positions. Thus, we can guess that BTO and STO tend to match their lattice constant (reducing a_{BTO} and increasing a_{STO}). Then, stress in each layer increases with period. The weak X-ray intensity

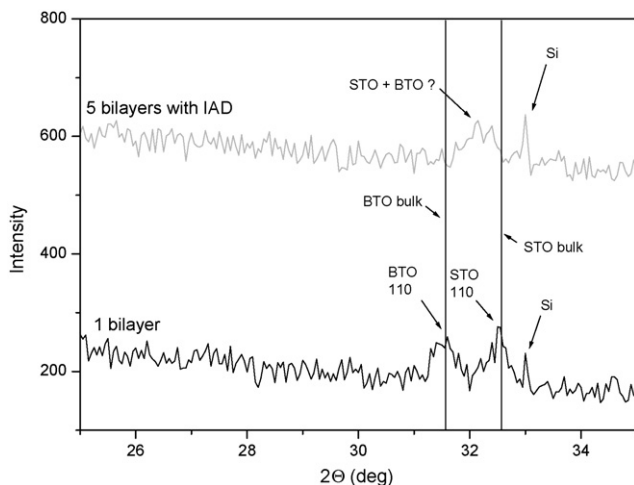


Fig. 1. XRD patterns θ - 2θ geometry of STO/BTO multilayers. One and 5 periods are plotted.

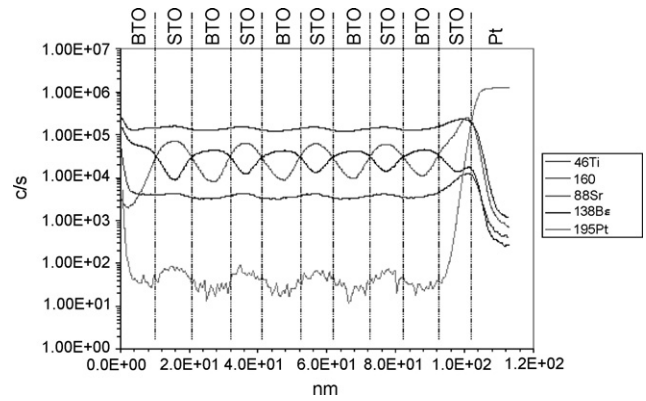


Fig. 2. SIMS plot of 5 periods STO/BTO after 625 °C anneal.

observed for all samples indicates that the long distance order is low.

Fig. 2 shows SIMS plots after a 625 °C annealing on the 5 periods sample. The 10 layers are clearly visible. However, slighter slopes than not-annealed sample (not represented here) are observed at the interfaces, which indicates that roughness or/and interdiffusion appear during annealing. Such results were already observed in literature, with 700 °C annealing on sol-gel deposited samples.⁶ This phenomenon is limited and this measurement proves that these samples are definitively different from a unique BST phase.

Fig. 3 shows TEM bright field picture for 5 periods crystallized films in sandwich between Pt electrodes. BTO layers are visible in darker contrast than STO. They are quite well defined which confirms the co-existence of distinct STO and BTO phases as observed by SIMS. The boundary between STO/BTO is less defined than BTO/STO one. This was already observed in literature for PLD technique and was explained by Visinoinu et al. as a difference of surface energies for STO and BTO.¹⁴ In our case, there is a technological difference between STO and BTO deposition: a secondary ion source sputters the sample during BTO deposition in order to obtain a stoichiometric film. STO

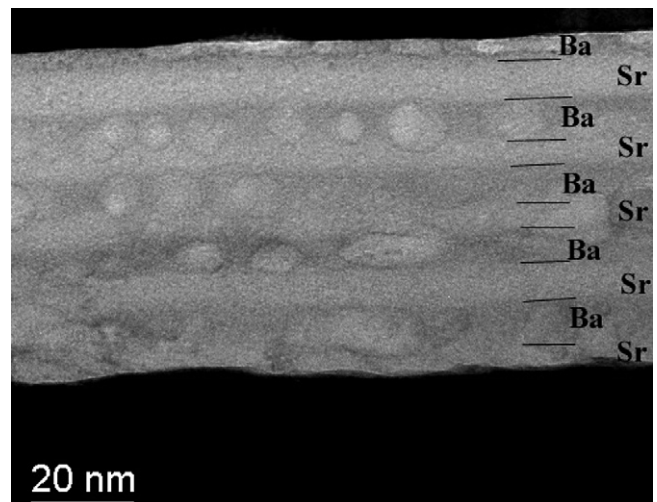


Fig. 3. TEM bright field images of crystallized samples. Five periods are represented.

deposition does not need this sample bombardment. Then, this secondary sputtering induces a STO/BTO interface roughness increase inducing a less defined interface.

The main drawback revealed by TEM is that BTO layers exhibit large spherical cavities having diameter that can be larger than BTO thickness. One notice that the last deposited BTO layer exhibit weaker cavities than “in-depth” BTO layers. This remark is valuable for all stacks realized in this study (1 and 2 periods not presented here). Holes in perovskite thin films were already observed after annealing, especially on PZT. The proposed explanation for PZT is that porosity is due to PbO exodiffusion. Indeed, PbO is the most volatile compound obtainable from PZT. A solution to avoid this phenomenon and then decrease porosity is to add Pb directly in the sputtering target. Some works show that better electrical results are obtained when PZT thin films exhibit a Pb excess.¹⁵ For our stacks, evaporation points of BaO and SrO (2000 and 3000 °C, respectively) are higher than annealing temperatures. Thus, holes observed in the stacks cannot be attributed to BaO loss. However, one can suppose that Ba diffuse in the STO layer as its mobility is higher than Sr.

3.2. Electrical results

High dielectric constant value, correlated with perovskite structure appears at 450 °C which is very interesting for Above IC integration. Fig. 4 represents the up and down capacitance and $\tan \delta$ losses versus voltage (C - V) curves of the 1, 2 and 5 periods stack annealed at 650 °C. An improvement in maximal permittivity is observed by increasing the number of periods: 56 for 1 period, 98 for 2 periods, and 102 for 5 periods. However, the dielectric constant remains quite low compared to literature. A first reason is that perovskite thin films dielectric constant is very sensitive to thickness. Here, they range between 65 and 85 nm. Let us note that STO and BTO single layers 100 nm-thick were realized and they exhibit dielectric constant value of 120 for STO and 150 for BTO, which is the same order of magnitude than multilayer stacks. The holes effect in BTO layers should

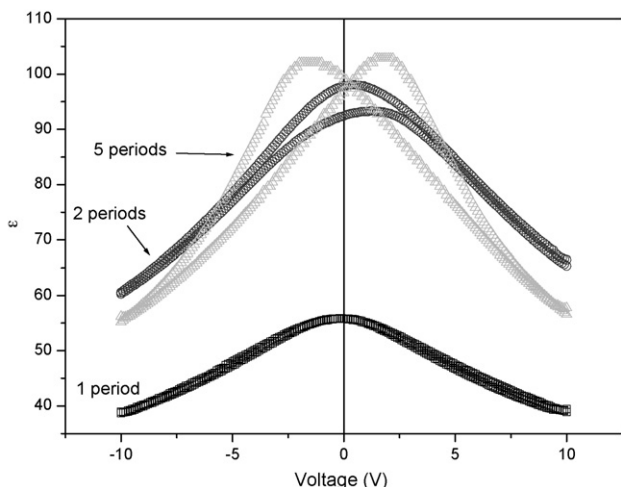


Fig. 4. C - V curves, up and down, of 1, 2 and 5 periods samples annealed at 650 °C.

be estimated more accurately. Finally, hysteresis behaviour is clearly seen for 5 periods curves in Fig. 4, which indicates a ferroelectric behaviour.

For RF and microwave applications, high tuning range of capacitance $TR = (C_{\max} - C)/C_{\max}$ versus DC voltage is needed. Concerning TR, it is noticeable that it increases with the number of periods. Values pointed calculated at -1 MV/cm are: 15% for 1 period, 21% for 2 periods and 37% for 5 periods. This involvement, such as permittivity involvement with period increase, was already seen in literature,¹⁶ and interpreted as interfaces strains. The fact that the 5 periods sample exhibits ferroelectric properties indicates the tuning range increase is certainly correlated with ferroelectricity.

Concerning the losses (not shown here), an improvement is visible with 5 periods stack. The $\tan \delta$ value obtained is less than 2% for that sample, whereas for 1 and 2 bilayers $\tan \delta$ exhibit values of 3 and 3.5%, respectively. From XRD results, it is observed that stacking a larger number of layers results in adding an internal stress in the films. As the dielectric properties (permittivity and losses) show improvement when period increases, one can conclude there is a strong correlation between internal stress and electrical behaviour.

Besides, increasing the number of periods leads to increase the ferroelectricity in the sample. As measured with Tower Sawyer circuit, remnant polarization P_r ranges from $0.5 \mu\text{C}/\text{cm}^2$ for 1 and 2 periods samples to $1.5 \mu\text{C}/\text{cm}^2$ for 5 periods sample. This behaviour is a drawback for the targeted application as no hysteresis is required for variable capacitance. However, the ferroelectric effect is weak and can be acceptable for some applications.

Another important property required for variable capacitors is a low temperature dependence of dielectric properties. Fig. 5 shows the relative dielectric constant K at 0 V of the STO/BTO stacks and the BTO single layer versus temperature in the 20–150 °C range, all samples being annealed at 600 °C. The first remark is that the temperature variation of K of all samples is very small compared to bulk materials. For BTO single layer, although the bulk Curie temperature is around 120 °C, the K also decreases in all the temperature ranges with a small peak

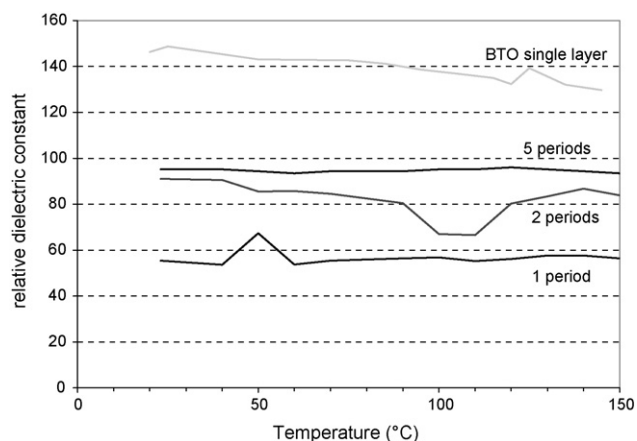


Fig. 5. Temperature dependence of relative dielectric constant for 1, 2 and 5 periods stacks and BTO single layer.

around 130 °C. Among all samples, the 5 periods stack exhibits the smallest K temperature dependence which is under 2.7% in this temperature range.

4. Conclusion

STO/BTO multilayers were deposited by ion beam sputtering onto platinized substrates. Three stacks were tested in the 65–85 nm range: 1, 2 and 5 bilayers. The XRD results show that an internal stress appeared for 5 period films. SIMS measurements indicates that there is weak species interdiffusion after annealing. That is confirmed by TEM bright field pictures, which exhibits also microstructural defects (spherical cavities) in BTO layers. Permittivity values obtained range from 56 to 102 for 1 and 5 periods stacks, respectively. The best results for losses are also found with 5 periods sample (less than 2%). Increasing periods leads to an improvement of permittivity and losses, due to the internal stress added in the layers. The 5 periods stack has a ferroelectric behaviour. Tuning range with a DC voltage also increases with periods. Finally, temperature dependence was measured for each thin film. The 5 periods stack appears to be weakly temperature dependant. Finally, the number of periods should be increased and BTO composition revised to avoid holes. Results obtained with these STO/BTO stacks are promising for tuneable integrated capacitors.

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